AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for fabricating a memory device comprising:

depositing a first dopant in a first region of a semiconductor substrate of said ~~a~~ memory device;

subsequent to said depositing said first dopant, performing ~~an~~ a first annealing process upon said semiconductor substrate, wherein said first annealing process diffuses said first dopant a pre-determined percentage of a first complete diffusion state;

subsequent to said performing said first annealing process, ~~performing a second~~ depositing ~~of~~ a second dopant in a second region of said semiconductor substrate; and

subsequent to said depositing said second dopant, performing a second annealing process upon said semiconductor substrate, wherein said second annealing process diffuses said first dopant to said first complete diffusion state and said second dopant to a second complete diffusion state.

2. (currently amended) The method as recited in Claim 1, wherein said depositing said first ~~a~~ dopant comprises creating ~~an~~ first impurity concentration in said first region of said ~~a~~ semiconductor substrate of ~~a~~ said flash memory device, and wherein said depositing of said second dopant comprises creating a second impurity concentration in said second region of said semiconductor substrate of said flash memory device.

3. (currently ameneded) The method as recited in Claim 1, wherein said depositing ~~a~~ said first dopant comprises depositing ~~a~~ said first dopant for a plurality of semiconductor devices in a periphery region of said memory device.

4. (currently amended) The method as recited in Claim 3, wherein said performing ~~a~~ said second dopant depositing comprises depositing ~~a~~ said second dopant for a plurality of memory cells in a core region of said semiconductor substrate of said memory device.

5. (original) The method as recited in Claim 4, wherein a plurality of parameters of said second annealing process are selected based upon an electrical characteristic of said plurality of memory cells.

6. (canceled)

7. (canceled)

8. (currently amended) A method for fabricating a flash memory device comprising:

performing a first partial annealing process upon a first dopant deposited in a first region of a semiconductor substrate of said flash memory device;

subsequent to said first annealing process, depositing a second dopant in a second region of said semiconductor substrate; and

subsequent to depositing said second dopant, performing a second annealing process wherein said first dopant ~~deposited in said first region~~ and said second dopant ~~deposited in said second region~~ are simultaneously annealed.

9. (currently amended) The method as recited in Claim 8, wherein said first region comprises a plurality of semiconductor devices disposed in a periphery region of said flash memory device and ~~comprising performing a~~ wherein said partial annealing process is performed upon said plurality of semiconductor devices, and

wherein said partial annealing process renders a partially annealed state of said semiconductor devices.

10. (currently amended) The method as recited in Claim 9, wherein said second region comprises a plurality of memory cells disposed in a core region of said flash memory device and ~~comprising performing a partial~~ wherein said second annealing process renders a completely annealed ~~annealing process upon~~ state of said plurality of memory cells and a complete annealed state of said plurality of semiconductor devices.

11. (original) The method as recited in Claim 10, wherein a plurality of parameters of said second annealing process are selected based upon an electrical characteristic of said plurality of memory cells.

12. (original) The method as recited in Claim 11, wherein a plurality of parameters of said partial annealing process are selected based upon an electrical characteristic of said plurality of semiconductor devices and upon said plurality of parameters of said second annealing process.

13. (currently amended) A method for fabricating a memory device comprising:

initiating a partial diffusion of a first dopant deposited in a first region of a semiconductor substrate of a memory device;

subsequent to said partial diffusion, depositing a second dopant in a second region of said semiconductor substrate; and

subsequent to depositing said second dopant, initiating a second diffusion of said first and second dopants wherein said first dopant ~~in said first region~~ is further diffused concurrent with the diffusion of said second dopant ~~in said second region~~.

14. (original) The method as recited in Claim 13, wherein said memory device is a flash memory device.

15. (original) The method as recited in Claim 13, wherein said first region comprises a plurality of semiconductor devices disposed in a periphery region of said memory device.

16. (original) The method as recited in Claim 15, wherein said second region comprises a plurality of memory cells disposed in a core region of said memory device.

17. (original) The method as recited in Claim 16, wherein a plurality of parameters of said second diffusion are selected based upon an electrical characteristic of said plurality of memory cells.

18. (original) The method as recited in Claim 17, wherein said partial diffusion and said second diffusion comprise a cumulative diffusion for said plurality of semiconductor devices.

19. (original) The method as recited in Claim 18, wherein a plurality of parameters of said cumulative diffusion are selected based upon an electrical characteristic of said plurality of semiconductor devices.